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Negative Differential Resistance in Carbon Nanotube Field-Effect Transistors with Patterned Gate Oxide

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ABSTRACT We demonstrate controllable and gate-tunable negative differential resistance in carbon nanotube field-effect transistors, at room temperature and at 4.2 K. This is achieved by effectively creating quantum dots along the carbon nanotube channel by patterning the underlying, high-κ gate oxide. The negative differential resistance feature can be modulated by both the gate and the drain-source voltage, which leads to more than 20% change of the current peak-to-valley ratio. Our approach is fully scalable and opens up a possibility for a new class of nanoscale electronic devices using negative differential resistance in their operation.

KEYWORDS: carbon nanotubes · field-effect transistors · negative differential resistance · hysteresis · quantum dot · oscillator · high-κ

The first demonstration of negative differential resistance (NDR) in an electronic device was made during the 1970s in a GaAs double barrier structure.[1] Since then NDR has been observed in a variety of devices[2] all the way down to molecular scale.[3,4] There is a great interest for NDR in decreasingly smaller devices, motivated by the desire to reach high device integration densities. Another driving force is the fact that the capacitance of the NDR element is proportional to its size, which if it is too large restricts the accessible device characteristics. Recently, there have been emerging carbon nanotube[5] (CNT) devices that exhibit NDR in their electrical characteristics due to many different phenomena, for example, chemical doping,[6] defects,[7] heterojunctions,[8] quantum dots between the metal contact and the CNT,[9] and bundled or multiwalled CNTs.[10,11] While these observations give hope that CNTs can be used as NDR components in future electronics, so far the appearance of NDR in CNT devices has been uncontrolled and not suitable for mass production. In this work, we show a method for controlled and reproducible induction of NDR in a CNT field-effect transistor (FET) by patterning the underlying high-κ gate dielectric. The patterning creates local areas with significant charge trapping within the dielectric as the gate voltage is varied. The accumulated charges in the oxide modulate the effective electric field sensed by the nanotube and create reproducible electric field variations on the nanometer scale. We use the modulated electric field to induce an n−p−n or p−n−p structure along the nanotube. The patterning here is done with the dielectric materials TiO_2 and HfO_2, both of which are considered by the semiconducting industry as interesting materials for the future. Our approach opens a possibility for a new class of nanoscale electronic devices using NDR: fast switching elements,[12] nanoscale amplifiers,[13] and high frequency oscillators[14] which operate well into the THz domain.

RESULTS AND DISCUSSION

We observe reproducible negative differential resistance in three individual CNT-FETs with a device structure as depicted in Figure 1. The CNT-FETs consist of single-walled CNTs contacted at their ends by drain and source electrodes of Pd, and gated by the underlying Si substrate. The gate oxide is made by atomic layer deposition (ALD) of high-κ oxides which are patterned to influence the local electronic properties of our transistors. A cross-section of our devices together with the patterned profile of the grown ALD layers is illustrated in Figure 1a. An atomic force microscope (AFM) image of the ALD structure together with a cross shaped AFM marker is also shown in Figure 1b. In the dark grooves, there is only a single layer of HfO_2 (20 nm) on top of the silicon wafer. Between the lines, ALD islands of TiO_2−HfO_2 (with nominal thicknesses of 0.5−1 nm) are grown. An AFM image of one of the CNT-FET devices (D1) together with a schematic of the

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Received for review February 2, 2010 and accepted May 24, 2010.

Published online June 4, 2010.
10.1021/nn100208v

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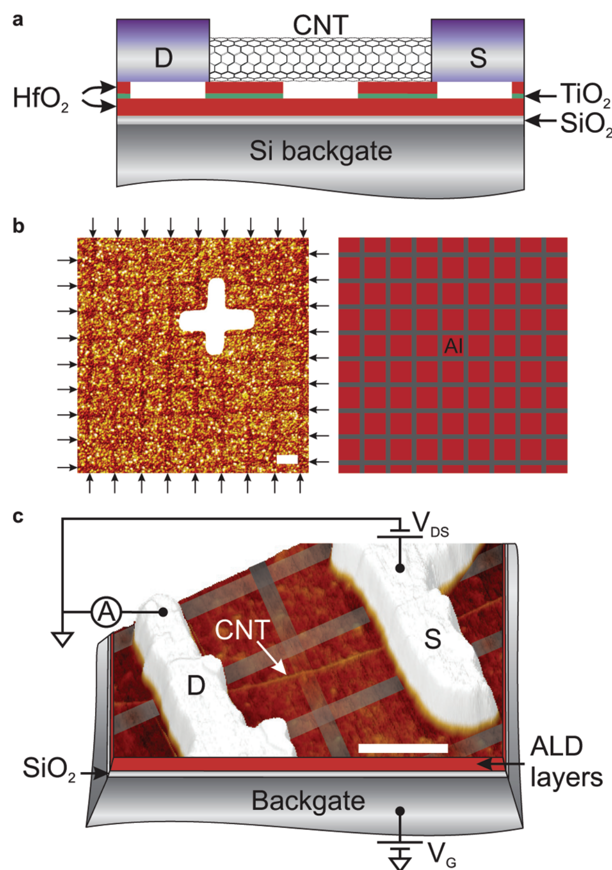

Figure 1. Integrating patterned gate oxide with CNT-FETs. (a) A schematic cross-section of our CNT-FETs having ALD grown triple layer of $HfO_2-TiO_2-HfO_2$ with patterned upper two layers of TiO_2-HfO_2. The nanotube is contacted with palladium (30 nm) drain (D) and source (S) electrodes. (b) An AFM image together with a schematic of ALD grown TiO_2-HfO_2 islands. In the grooves highlighted with arrows, there is a single layer of HfO_2 (20 nm) and between these grooves are additional layers of TiO_2-HfO_2 (0.5−1 nm) forming squares of *ca*. 200 nm × 200 nm (called ALD islands in the following). The width of the groove between the islands is measured with AFM to be ~50 nm. Also an AFM marker is visible in the image. (c) An AFM image of device D1 where a SWCNT is connected to drain (D) and source (S) electrodes having channel length of ~400 nm. Also the measurement setup is schematically illustrated. Between the CNT and the gate we have the ALD island structure. Scale bars are 200 nm.

measurement setup and the ALD islands is shown in Figure 1c.

The purpose of patterning the ALD-grown gate oxide is to create controlled charge trapping at specific places within the gate oxide.[15] With sufficient gate voltages the patterned charge trapping induces p−n junctions along the channel of the CNT-FET. The p−n junctions can be used to create well-defined quantum dots along the CNT. A quantum dot that is properly gated in relation to its semiconducting contact leads may display band-to-band tunneling[16] accompanied by NDR as the drain-source bias is swept across discrete levels within the dot. We find that in our devices, NDR appears for gate voltages in the vicinity of the CNT band gap, which is in good agreement with having band-to-band tunneling. Further evidence of p−n junction confinement in our devices is found in the bipolar behavior in the transfer characteristics of all our CNT-FETs, as well as a specific quantum dot behavior at 4.2 K.

An earlier study found NDR in freely suspended nanotubes, and showed that it was induced at relatively large bias voltages due to self-heating and increased electron−phonon scattering.[17] This is not the case in our devices, since the nanotube rests on and is thermalized by the substrate. A more likely cause for the emergence of NDR is that a resonant tunneling level enters into the drain-source bias window. This is illustrated in detail in the form of a differential conductance plot in Figure 2a measured for device D2, at 4.2 K. The NDR is visible with both positive and negative drain-source voltages as diagonal lines that occur after a resonant level enters to the bias window, as highlighted with arrows. For positive drain-source bias we observe strong NDR peaks related to two resonant levels. Also the charging of the gate oxide is visible in the images as abrupt horizontal displacements of the slopes while sweeping the gate voltage. The inset of Figure 2a shows that the NDR emerges in the vicinity of the band gap edge of the CNT.

In Figure 2b, the first NDR feature is increased only slightly while changing the gate to more positive voltages, whereas the second NDR feature has a 20-fold increase. These results show that the place of the NDR and more importantly its magnitude are tunable with the gate voltage (for more discussion, see Supporting Information). Moreover, our approach to induce NDR to CNT-FETs is fully scalable, and the islands providing the effect can be accurately positioned at any desired location on the underlying wafer.

The inset of Figure 2b shows two typical current *vs* drain−source voltage curves, both measured on device D1 in 1.3×10^{-2} mbar vacuum at room temperature and at 4.2 K. Clear NDR peaks are visible in both traces, situated at around −0.3 V at room temperature and around −0.18 V at 4.2 K. The difference between the peak and the valley current is ~3.5 nA at room temperature and ~4 nA for the same device measured in cold. In this study, we had in total three large-band gap CNT-FETs with good transistor characteristics. All of them show clear and reproducible NDR. While the sample pool is small, the consistency points toward a high yield for creating NDR in semiconducting CNTs with our patterned gate oxide method. The phenomenon observed here is different from multimode (multisubband) effects observed in refs 18 and 19 because multimode effects produce steps (or plateaus) in I_D-V_{DS} and I_D-V_G characteristics, not peaks and NDR as in Figure 2. The phenomenon is rather related to band-to-band tunneling,[16] where resonant tunneling from the valence into the conduction band and *vice versa* enables the flow of current through the device as described below.

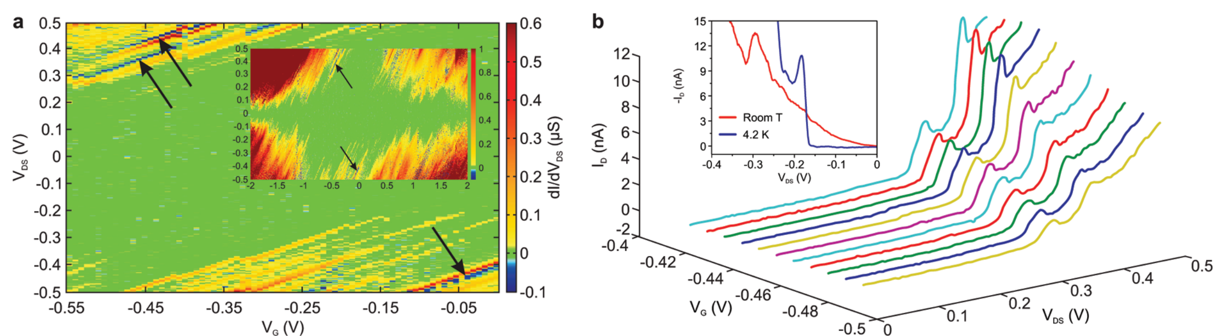

Figure 2. Negative differential resistance in gate-oxide designed CNT-FETs. (a) Differential conductance for device D2 measured at 4.2 K. The NDR regions are shown with blue and indicated with arrows. NDR is visible at both positive and negative drain−source bias voltages. At positive bias the NDR is related to two different resonant tunneling levels. In the inset is shown a larger parameter space from the same device. The NDR occurs in the vicinity of the CNTs band gap as indicated by arrows. (b) The development of the NDR related to the two resonant levels. When sweeping the gate to more positive voltages, the NDR corresponding to the first resonant level increases only slightly while the NDR related to the second localized level has a 20-fold increase. Inset: Current *vs* voltage curves for the device D1 measured at room temperature (red) and at 4.2 K (blue). Clear NDR peaks are visible for both, situated at around −0.3 V at room temperature and around −0.18 V at 4.2 K. The peak to valley ratio is 1.38 for room temperature and 1.45 at 4.2 K. The gate voltage sweep direction was from negative to positive.

We explain the observations by the formation of p−n junctions in the middle of the CNT due to specific and efficient charging of the ALD islands, effectively forming quantum dots in the CNT[20] whose resonant tunneling levels enable the NDR phenomenon.[21] This is schematically illustrated in Figure 3. With zero gate voltage, the ALD islands are neutral (Figure 3a), corresponding to the flat band case. When the gate voltage is increased, electrons from the CNT tunnel to the ALD islands, making them charged (Figure 3b). The charge stored within the islands screens the applied gate voltage. Thus, the sections of the CNT above these regions, forming the CNT drain and source sections, see a smaller electric field. On the other hand, the region between the islands stays uncharged and in this region the positive gate voltage can lower the bands in energy. When a sufficiently high voltage is applied to the gate, the CNT band gap descends below the Fermi level (E_F) and forms an n-type quantum dot with discrete electronic states. At a fixed gate voltage, with increasing amplitude of the drain voltage, the current increases at first, until a resonant tunneling level aligns with the Fermi level and the current reaches a local maximum. When further increasing the amplitude of the drain voltage, the resonant level moves below the Fermi level of the p-type CNT drain section and the current drops, until the next resonant level enters to the bias window. If the gate voltage would subsequently be lowered from a high value, the accumulated charge on the ALD islands will remain largely unaffected, until the gate polarity has changed and reached some threshold value at which the tunneling of electrons is driven the opposite way. So when the gate voltage is made more negative, the electrons stored in the ALD islands feel this negative potential and tunnel out from the islands, leaving the islands positively charged.[22] The islands will then stay positively charged until a sufficiently large positive gate voltage will aid electrons to tunnel back. This makes overscreening possible and the ends of the CNT become n-type although the backgate voltage is still negative. As in the case of forming an n-type quantum dot, the region between the islands stays uncharged, and in this region the negative gate voltage can hoist the bands in energy forming a p-type quantum dot (Figure 3c).

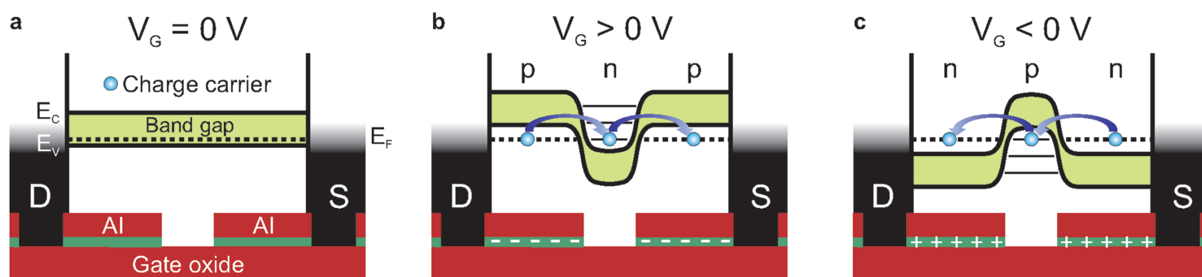

Figure 3. Quantum dots defined by charging the ALD island structure. (a) The flat band case at zero gate voltage. The Fermi level (E_F) within the band gap of the CNT is aligned with the drain (D) and source (S) electrodes and the ALD islands are neutral. (b) A positive gate voltage pulls electrons from the CNT to the ALD islands which in turn screens the applied V_G. Between the islands, the oxide stays uncharged and the conductance band (E_C) is pulled below the Fermi level. The resulting p−n junctions define a quantum dot with discrete electronic states. When a resonant level is aligned with the Fermi level the charge carriers can flow. (c) The electrons are ejected from the ALD islands by applying a negative gate voltage and the remaining positive charge screens the V_G above these sections. Between these islands, the valence band (E_V) is pulled above the Fermi level and the resulting p−n junctions form a quantum dot.

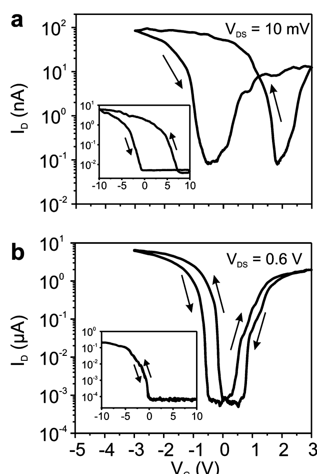

Figure 4. Hysteresis and ambipolar behavior of CNTs on ALD islands compared to CNTs on SiO_2. (a) Transfer characteristics at room temperature with V_{DS} = 10 mV showing advanced hysteresis. The subthreshold slopes are for p-type ~89 mV/dec and for n-type ~161 mV/dec. Repeated I−V_G scans are shown in Supporting Information. In the inset is shown hysteresis in a CNT-FET having commonly used SiO_2 as a gate oxide (for more discussion, see Supporting Information). (b) Hysteresis at 4.2 K with V_{DS} = 0.6 V. The relative hysteresis decreases by 80% compared to the original room temperature hysteresis but it still remains strong. The corresponding subthreshold slopes are for p-type ~17 mV/dec and for n-type ~49 mV/dec. Repeated I−V_G scans are shown in Supporting Information. In the inset is shown hysteresis in a CNT-FET having commonly used SiO_2 as a gate oxide (for more discussion, see Supporting Information).

The sample geometry and NDR mechanism is analogous to the negative differential resistance observed in double barrier structures like GaAs quantum dots.[1,23,24] The formation of n−p−n or p−n−p junctions in CNTs can in a similar way be achieved through the use of locally placed gates in addition to the large gate formed by the substrate. The local gates can either be buried in the substrate dielectric beneath the CNT[25,20] or placed on top of the CNT with a suitable dielectric layer in between.[26−28] While NDR has been observed for such devices,[25] the reproducibility and scalability is more limited due to additional processing steps and the need to leave space for the gate interconnects. This kind of sample has so far mainly been used to study aspects other than NDR, such as CNT-FET operation limits,[28] interaction between quantum dots,[27,20] and quantum capacitance.[29]

In our earlier work,[15,30] we showed that ALD grown nanometer thick gate oxides of high-κ materials such as HfO_2, and layer structures such as HfO_2−TiO_2−HfO_2, are an efficient way to create controllable charge trapping in CNT devices. To further demonstrate that we have significant charge trapping here, we will point out a few observations from gate dependence measurements. We observe bipolar transconductance curves (Figure 4) for all the devices with the patterned gate oxide (ALD islands). This indicates that both the valence and conduction bands are contributing to the transconductance and make band-to-band tunneling plausible.[16] Control experiments with SiO_2 backgated CNT-FETs do not show bipolar transconductance (Figure 4a,b,insets). The devices have very steep subthreshold slopes, down to 89 mV/dec at room temperature and 17 mV/dec at 4.2 K. While not reaching below the thermal limit, which has been shown possible when having band-to-band tunneling,[16] these values are well comparable with other studies where band-to-band tunneling was attributed to highly performing CNT transistors.[28] There is a variation of the subthreshold slope with temperature, which is not expected for a pure band-to-band tunneling scenario.[16] But the temperature dependence of the subthreshold slope may as well come from the temperature dependent charging within the dielectric, which visibly changes the hysteresis in Figure 4. The persistent advanced hysteresis at low temperatures in Figure 4b shows that we have in these devices very strong charge trapping within the oxide (for more discussion, see Supporting Information). The smaller hysteresis at low temperatures is consistent with a smaller amount of charging. That in turn gives a less efficient screening of the gate, resulting in a steeper subthreshold slope. Here we would like to emphasize that the charge trapping is a stationary state in the ALD islands, induced by the gate voltage in a preparatory step in the negative differential resistance measurement, and it does not participate in the (possibly ultrafast) dynamics driven by the drain−source voltage. The charges are not dynamically moving in the steady state but can be preserved in the gate oxide for hours.[15,30] Thus, the high frequency characteristics of the devices are not affected by the charge trapping. For comparison, we also measured reference samples having uniform, *nonpatterned* conventional SiO_2 and an ALD grown triple layer of HfO_2−TiO_2−HfO_2 as their gate oxides (see Supporting Information). While they showed similar results for hysteresis at room temperature (inset of Figure 4a) and the triple layer reference sample also at 4.2 K, the SiO_2 reference sample did not show any hysteresis at 4.2 K (inset of Figure 4b). And most importantly, for both of these reference samples without the ALD island structure, we did not observe any NDR (see Supporting Information).

To quantitatively test how well the p−n junction and quantum dot model can explain the observed NDR, we estimate the expected energy level separation in the quantum dots formed by the ALD islands. From the AFM images shown in Figure 1b,c we can estimate the quantum dot size for D1 to be ~60 nm. In the constant interaction model,[31] the electrochemical potentials of transitions between successive resonant tunneling levels in a quantum dot are spaced by the so-called addition energy $E_{add} = \Delta E + E_C$ where E_C is the charging energy and ΔE is the energy spacing between two discrete quantum levels. For our system we obtain a level splitting of $\Delta E \approx 14$ meV and a charging energy of $E_C \approx 6$ meV (see Supporting Information); that is,

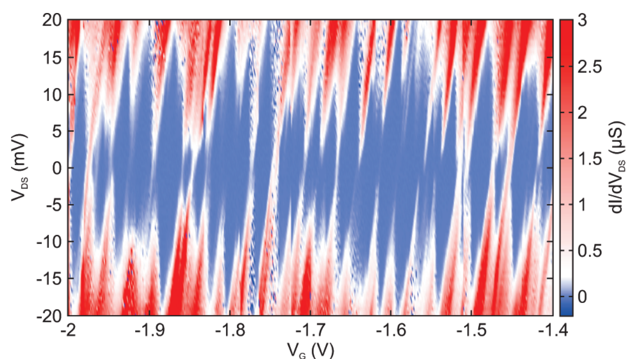

Figure 5. Stability diagram of the n-p-n quantum dot. At 4.2 K, Coulomb blockade is visible in a series of diamonds and corresponds to a single electron charging of a quantum dot of the size ~60 nm, having an addition energy ~20 meV. The gate voltage sweep direction was from negative to positive.

$E_{add} \approx$ 20 meV. This estimation of the addition energy fits remarkably well to our measured stability diagram for D1 in Figure 5, showing characteristic Coulomb blockade. These values are also significantly lower than the CNT subband separations of several hundreds of meV based on our CNT diameter range of 1.3−3.4 nm,[32] which speaks against the involvement of multimode effects. In addition, we do not observe the tunneling barriers to tune to transparency at any backgate voltage in any of the three devices, as was shown in the case of quantum dot formation by defects in CNTs.[33] Some of the diamonds are abruptly cut, supporting the conclusion that we have strong charging within the dielectric in these devices.

CONCLUSIONS

We have presented a new technique to induce negative differential resistance in carbon nanotube field-effect transistors at room temperature. By patterning the upper two layers of ALD grown HfO_2−TiO_2−HfO_2 triple layer gate oxide into separate islands, we can control the charging within the gate oxide and induce NDR by forming a quantum dot in the conduction channel of the CNT-FET. With gate voltage we can control the magnitude and the place where the NDR occurs in V_{DS}. The advantages of our method over the introduction of quantum dots with more commonly used local gates are as follows: (1) Our method is fully scalable, since the islands providing the screening effect can be accurately positioned at any desired location on the underlying wafer. (2) When a quantum dot is already induced to the conduction channel of the CNT, using charging of the ALD islands, there is no need to use gate voltages to sustain the situation, which is not the case in a device with metallic local gates. (3) Also the accurate placement of the CNT is not needed in our approach, since the CNTs can be positioned freely anywhere on the ALD islands.

Our method can also be used to generate NDR in other materials such as graphene or nanowires. The essential requirement here for semiconducting channel material is to have a suitable size band gap which forms the tunneling barriers in the quantum dot, induced by the screening of the gate voltage with the ALD islands in the source and drain sections of the channel material. Suitable materials include, for example, graphene nanoribbons and silicon nanowires.

Our novel technique enables a new class of low-cost nanoscale devices using NDR in their operation. Theoretical predictions of oscillations through CNT quantum dots with NDR suggest they could reach tens of terahertz (THz) with output powers of several microwatts (μW).[14] Both parameters supersede the intrinsic limitations of state-of-the-art RTD oscillators made with conventional semiconductor technology, with current record of 712 GHz by an InAs/AlSb resonant-tunneling diode with an output power of 0.3 μW.[34,35] While our presented prototypes have resistance values that limit the upper frequency to around 50 GHz, with a by-all-means realistic reduction of the CNT-to-electrode contact resistance to below 10 kΩ and the NDR resistance to below 100 kΩ, the terahertz mark would be reached (see Supporting Information). It has also been suggested that the output power of high frequency oscillators could be increased into the milliwatt range, by combining several devices either in series[36] or parallel[14] configuration, depending on how the signal is coupled out. Our method of inducing NDR in CNT-FETs is suitable for both configurations, in particular the series integration which can be done along one single CNT, and may provide a path to making the first continuous wave oscillator that works well into the terahertz domain.

MATERIALS AND METHODS

The devices were built on a highly boron-doped Si wafer, which also served as a backgate. Without removing the native SiO_2 layer from the surface, an ALD deposition of the first HfO_2 layer was carried out on top of the wafer by Beneq Oy (Vantaa, Finland), using a Beneq P400A ALD deposition tool. Precursors of hafnium tetrachloride ($HfCl_4$) and water were used at a deposition temperature of 300 °C. The thickness of this layer, 20 ± 1 nm, and its refractive index of 2.05 ± 0.01, was measured with a Rudolph Research AutoEL III ellipsometer with an excitation wavelength of 632.8 nm. Next a matrix of alignment markers of Pd (25 nm) with an adhesion layer of Ti (5 nm) was deposited, using e-beam lithography and metallization. Subsequently a second e-beam lithography step was done to open squares in the poly(methyl methacrylate) (PMMA) with nominal dimensions of 150 nm × 150 nm. Here also optical lithography or nanoimprint lithography could be used. Then another ALD deposition together with a lift-off procedure was performed to produce more than 20 000 ALD islands comprising TiO_2−HfO_2, having nominal thicknesses of 0.5 and 1 nm, respectively. The total thickness of this oxide stack is measured with AFM to be ~0.5 nm. The heights of the ALD islands are smaller than the radius of the studied tubes which makes it unlikely to induce any suspended sec-

tion in the CNTs.[37−39] Precursors used were titanium tetrachloride ($TiCl_4$) and water for TiO_2 growth and tetrakis(ethylmethylamino)hafnium (TEMA-Hf) and water for HfO_2 growth, both done at a deposition temperature of 100 °C. These ALD grown oxides were chosen due to the specific charge trapping within the oxide stack,[15] ease of patterning of the oxides, and high control of the properties of the oxides with the ALD process.[40,41]

A few droplets of nanotube suspension made in 1,2-dichloroethane by ultrasonication, containing commercial single-walled carbon nanotubes (SWCNTs) bought from NanoCyl S.A. (Sambreville, Belgium), was then deposited onto the sample. The locations of the CNTs were precisely mapped in relation with the alignment marker matrix using an atomic force microscope in the tapping mode, which does not deform the CNTs. Chosen CNTs were then contacted with drain (D) and source (S) electrodes of Pd (30 nm) through a third e-beam lithography step and subsequent metallization. On the basis of AFM images, the FET channel lengths in this study were 400 ± 10 nm and the diameters of the individual CNTs ranged from 1.3 to 3.4 nm, corresponding to single nanotubes rather than bundles. (See Supporting Information for the diameter dependence of NDR.) The silicon wafer is used as a backgate for three-terminal operation. The drain−source and gate−source voltage bias was supplied for all the measurements from a homemade voltage distribution box powered by batteries and computer-controlled *via* a data acquisition card. The room temperature measurements were done at ambient conditions as well as in vacuum for reducing surface chemistry effects such as adsorbed water. Vacuum measurements were done in a homemade vacuum chamber at a pressure of 1.3×10^{-2} mbar. The liquid helium measurements at 4.2 K were done with a homemade dipstick, where the sample was situated in a helium atmosphere of a few mbar, isolated from the liquid helium. All measurements were carried out in an electrically shielded room.

Acknowledgment. We acknowledge valuable discussions with our research project collaborators: the research groups of M. Ahlskog, K. Rissanen, and J. J. Toppari at the University of Jyväskylä, E. I. Kauppinen's group at Helsinki University of Technology, and the companies Nokia Oyj and Vaisala Oyj. We thank Beneq Oy, O. Jylhä for ALD processing. This work was supported by the Finnish Funding Agency for Technology and Innovation (TEKES), Project No. 40309/05, and by the Academy of Finland (Project Nos. 213362, 217045, 217041) and conducted as part of a EURYI scheme award (see www.esf.org/euryi). M.R. would like to acknowledge support from the Magnus Ehrnrooth Foundation and the Finnish Foundation for Technology Promotion (TES).

Supporting Information Available: Results on reference samples having either SiO_2 or $HfO_2-TiO_2-HfO_2$ triple-layer gate oxide; estimation of the energy level separation in the quantum dots together with estimations of the cutoff frequency, the output power of NDR-based oscillators, and Fermi level position in the flat band case; diameter dependence of the NDR feature; the controlled modulation of the NDR feature. This material is available free of charge *via* the Internet at http://pubs.acs.org.

REFERENCES AND NOTES

1. Chang, L. L.; Esaki, L.; Tsu, R. Resonant Tunneling in Semiconductor Double Barriers. *Appl. Phys. Lett.* **1974**, *24*, 593–595.
2. Capasso, F.; Sen, S.; Gossard, A. C.; Spah, R. A.; Hutchinson, A. L.; Chu, S. N. G. Observation of Resonant Tunneling Through a Compositionally Graded Parabolic Quantum Well. *IEEE Int. Electron. Dev. Meet.* **1987**, *33*, 66–69.
3. Chen, J.; Reed, M. A.; Rawlett, A. M.; Tour, J. M. Large On−Off Ratios and Negative Differential Resistance in a Molecular Electronic Device. *Science* **1999**, *286*, 1550–1552.
4. Zeng, C.; Wang, H.; Wang, B.; Yang, J.; Hou, J. G. Negative Differential-Resistance Device Involving Two C60 Molecules. *Appl. Phys. Lett.* **2000**, *77*, 3595–3597.
5. Charlier, J.-C.; Blase, X.; Roche, S. Electronic and Transport Properties of Nanotubes. *Rev. Mod. Phys.* **2007**, *79*, 677–732.
6. Zhou, C.; Kong, J.; Yenilmez, E.; Dai, H. Modulated Chemical Doping of Individual Carbon Nanotubes. *Science* **2000**, *290*, 1552–1555.
7. Buchs, G.; Ruffieux, P.; Groning, P.; Groning, O. Defect-Induced Negative Differential Resistance in Single-Walled Carbon Nanotubes. *Appl. Phys. Lett.* **2008**, *93*, 073115.
8. Chandra, B.; Bhattacharjee, J.; Purewal, M.; Son, Y.-W.; Wu, Y.; Huang, M.; Yan, H.; Heinz, T. F.; Kim, P.; Neaton, J. B.; Hone, J. Molecular-Scale Quantum Dots from Carbon Nanotube Heterojunctions. *Nano Lett.* **2009**, *9*, 1544–1548.
9. Lee, S. W.; Kornblit, A.; Lopez, D.; Rotkin, S. V.; Sirenko, A. A.; Grebel, H. Negative Differential Resistance: Gate Controlled and Photoconductance Enhancement in Carbon Nanotube Intraconnects. *Nano Lett.* **2009**, *9*, 1369–1373.
10. Li, J.; Zhang, Q. Room-Temperature Negative Differential Conductance in Carbon Nanotubes. *Carbon* **2005**, *43*, 667–670.
11. Ahlskog, M.; Herranen, O.; Johansson, A.; Leppäniemi, J.; Mtsuko, D. Electronic Transport in Intermediate-Sized Carbon Nanotubes. *Phys. Rev. B* **2009**, *79*, 155408.
12. Haddad, G. I.; Mazmunder, P. Tunneling Devices and Applications in High Functionality/Speed Digital Circuits. *Solid-State Electron.* **1997**, *41*, 1515–1524.
13. Laskar, J.; Ketterson, A. A.; Baillargeon, J. N.; Brock, T.; Adesida, I.; Cheng, K. Y.; Kolodzey, J. Gate-Controlled Negative Differential Resistance in Drain Current Characteristics of AlGaAs/InGaAs/GaAs Pseudomorphic MODFETs. *IEEE Electron Dev. Lett.* **1989**, *10*, 528–530.
14. Dragoman, D.; Dragoman, M. Terahertz Oscillations in Semiconducting Carbon Nanotube Resonant-Tunneling Diodes. *Phys. E* **2004**, *24*, 282–289.
15. Rinkiö, M.; Johansson, A.; Zavodchikova, M. Y.; Toppari, J. J.; Nasibulin, A. G.; Kauppinen, E. I.; Törmä, P. High-Yield of Memory Elements from Carbon Nanotube Field-Effect Transistors with Atomic Layer Deposited Gate Dielectric. *New J. Phys.* **2008**, *10*, 103019.
16. Appenzeller, J.; Lin, Y.-M.; Knoch, J.; Avouris, P. Band-to-Band Tunneling in Carbon Nanotube Field-Effect Transistors. *Phys. Rev. Lett.* **2004**, *93*, 196805.
17. Pop, E.; Mann, D.; Cao, J.; Wang, Q.; Goodson, K.; Dai, H. Negative Differential Conductance and Hot Phonons in Suspended Nanotube Molecular Wires. *Phys. Rev. Lett.* **2005**, *95*, 155505.
18. Antonov, R. D.; Johnson, A. T. Subband Population in a Single-Wall Carbon Nanotube Diode. *Phys. Rev. Lett.* **1999**, *83*, 3274–3276.
19. Appenzeller, J.; Knoch, J.; Radosavljevic, M.; Avouris, Ph. Multimode Transport in Schottky-Barrier Carbon-Nanotube Field-Effect Transistors. *Phys. Rev. Lett.* **2004**, *92*, 226802.
20. Steele, G. A.; Gotz, G.; Kouwenhoven, L. P. Tunable Few-Electron Double Quantum Dots and Klein Tunnelling in Ultraclean Carbon Nanotubes. *Nat. Nanotechnol.* **2009**, *4*, 363–367.
21. Léonard, F.; Tersoff, J. Multiple Functionality in Nanotube Transistors. *Phys. Rev. Lett.* **2002**, *88*, 258302.
22. Zhao, C. Z.; Zhang, J. F.; Chang, M. H.; Peaker, A. R.; Hall, S.; Groeseneken, G.; Pantisano, L.; De Gendt, S.; Heyns, M. Stress-Induced Positive Charge in Hf-Based Gate Dielectrics: Impact on Device Performance and a Framework for the Defect. *IEEE Trans. Electron Devices* **2008**, *55*, 1647–1655.
23. Sollner, T. C. L. G.; Goodhue, W. D.; Tannenwald, P. E.; Parker, C. D.; Peck, D. D. Resonant Tunneling Through Quantum Wells at Frequencies up to 2.5 THz. *Appl. Phys. Lett.* **1983**, *43*, 588–590.
24. Reed, M. A.; Randall, J. N.; Aggarwal, R. J.; matyi, R. J.; Moore, T. M.; Wetsel, A. E. Observation of Discrete Electronic States in a Zero-Dimensional Semiconductor Nanostructure. *Phys. Rev. Lett.* **1988**, *60*, 535–537.

25. Cao, J.; Wang, Q.; Wang, D.; Dai, H. Suspended Carbon Nanotube Quantum Wires with Two Gates. *Small* **2005**, *1*, 138–141.
26. Javey, A.; Kim, H.; Brink, M.; Wang, Q.; Ural, A.; Guo, J.; McIntyre, P.; McEuen, P. L.; Lundstrom, M.; Dai, H. High-κ Dielectrics for Advanced Carbon-Nanotube Transistors and Logic Gates. *Nat. Mater.* **2002**, *1*, 241–246.
27. Mason, N.; Biercuk, M. J.; Marcus, C. M. Local Gate Control of a Carbon Nanotube Double Quantum Dot. *Science* **2004**, *303*, 655–658.
28. Javey, A.; Tu, R.; Farmer, D. B.; Guo, J.; Gordon, R. G.; Dai, H. High Performance *n*-Type Carbon Nanotube Field-Effect Transistors with Chemically Doped Contacts. *Nano Lett.* **2005**, *5*, 345–348.
29. Ilani, S.; Donev, L. A. K.; Kindermann, M.; McEuen, P. L. Measurement of the Quantum Capacitance of Interacting Electrons in Carbon Nanotubes. *Nat. Phys.* **2006**, *2*, 687–691.
30. Rinkiö, M.; Johansson, A.; Paraoanu, G. S.; Törmä, P. High-Speed Memory from Carbon Nanotube Field-Effect Transistors with High-κ Gate Dielectric. *Nano Lett.* **2009**, *9*, 643–647.
31. Hanson, R.; Kouwenhoven, L. P.; Petta, J. R.; Tarucha, S.; Vandersypen, L. M. K. Spins in Few-Electron Quantum Dots. *Rev. Mod. Phys.* **2007**, *79*, 1217–1265.
32. Saito, R.; Dresselhaus, G.; Dresselhaus, M. S. Trigonal Warping Effect of Carbon Nanotubes. *Phys. Rev. B* **2000**, *61*, 2981.
33. Bockrath, M.; Liang, W.; Bozovic, D.; Hafner, J. H.; Lieber, C. M.; Tinkham, M.; Park, H. Resonant Electron Scattering by Defects in Single-Walled Carbon Nanotubes. *Science* **2001**, *291*, 283–285.
34. Nishizawa, J.; Potka, P.; Kurabayashi, T. Ballistic and Tunneling GaAs Static Induction Transistors: Nano-Devices for THz Electronics. *IEEE Trans. Electron Dev.* **2002**, *49*, 1102–1111.
35. Brown, E. R.; Söderström, J. R.; Parker, C. D.; Mahoney, L. J.; Molvar, K. M.; McGill, T. C. Oscillations Up to 712 GHz in InAs/AlSb Resonant-Tunneling Diodes. *Appl. Phys. Lett.* **1991**, *58*, 2291–2293.
36. Yang, C. C.; Pan, D. Theoretical Investigations of a Proposed Series Integration of Resonant Tunneling Diodes for Millimeter-Wave Power Generation. *IEEE Trans. Microwave Theory Tech.* **1992**, *40*, 434–441.
37. Hertel, T.; Walkup, R. E.; Avouris, P. Deformation of Carbon Nanotubes by Surface van der Waals Forces. *Phys. Rev. B* **1998**, *58*, 13870.
38. Walkeajärvi, T.; Lievonen, J.; Ahlskog, M.; Åstrom, J.; Koshio, A.; Yudasaka, M.; Iijima, S. Bending of Multiwalled Carbon Nanotubes over Gold Lines. *J. Appl. Phys.* **2005**, *98*, 104301–4.
39. Janssen, J. W.; Lemay, S. G.; Kouwenhoven, L. P.; Dekker, C. Scanning Tunneling Spectroscopy on Crossed Carbon Nanotubes. *Phys. Rev. B* **2002**, *65*, 115423.
40. Puurunen, R. L. Surface Chemistry of Atomic Layer Deposition: A Case Study for the Trimethylaluminum/Water Process. *J. Appl. Phys.* **2005**, *97*, 121301.
41. Knez, M.; Nielsch, K.; Niinistö, L. Synthesis and Surface Engineering of Complex Nanostructures by Atomic Layer Deposition. *Adv. Mater.* **2007**, *19*, 3425–3438.